Title	: Sorting Objects Having Variable Length Keys		
Inventors:	Christopher Y. Blaicher		
Serial No :	10/618,500	Docket :	149-0105US
Mail Stop:	AF	Customer :	29855

REPLY TO FINAL OFFICE ACTION DATED 15 MAY 2006

This paper is intended to be a complete response to the above-identified Office Action. It is believed no fee is due. If fees are required, however, the Commissioner is authorized to deduct the necessary charges from Deposit Account 501922/149-0105US.

No claims have been added, cancelled or amended in this Reply. Accordingly, claims 1-63 are currently pending.

Acknowledgement of Prior Actions

Assignee notes with appreciation that the Examiner has accepted Assignee's prior filed specification amendments and that these amendments overcome the Examiner's prior rejections related to the drawings. Office Action at page 2 (¶ 3) and page 3 (¶ 4).

Section 103 Rejections based on Applicants Admitted Prior Art and Matsuda et al.

The Examiner has rejected claims 1-12, 16-24, 27-37 and 40-52 as allegedly being unpatentable under 35 U.S.C. 103(a) over Applicant's Admitted Prior Art (hereinafter AAPA) in view of U.S. Patent 5,247,665 to Matsuda et al. (hereinafter Matsuda). Specifically, the Examiner asserts that:

> With respect to independent claims 1, 16, 27 and 40, AAPA teaches all of the claimed elements except "wherein the expanded key information is not stored in intermediate storage." The Examiner cites to Matsuda at Abstract and col. 6, lines 52-67 and Figure 2, alleging that "[t]hese lines and fig 2 discloses the extraction and expansion of the key fields by adding the addresses of main memory. These expanded keys are not being stored in any intermediate storage but are being stored in the main memory." Office

> Action at page 5. The Examiner concludes by stating that "[i]t would have been obvious to one or ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because Mastuda's teaching would have allowed AAPA to reduce the load factors of the CPU and bus system and the processing performance is greatly improved by not transferring the result from the magnetic disk/intermediate storage (Matsuda Col 7, Lines 36-40)." Office Action at page 5 (¶ 5).

1. US 5,247,665 to Matsuda et al. ("Matsuda")

Matsuda appears to describe ten (10) embodiments of a database processing apparatus for, *inter alia*, perform sorting operations in a relational database ("RDB"). Matsuda at Abstract, 1:62-2:2, 2:3-33 (first embodiment), 2:34-3:2 (second embodiment), 3:3-22 (third embodiment), 3:23-56 (fourth embodiment), 3:57-4:24 (fifth embodiment), 4:25-59 (sixth embodiment), 4:60-5:25 (seventh embodiment), 5:26-64 (eighth embodiment), 5:65-6:35 (ninth embodiment) and 6:36-7:17 (tenth embodiment). It appears the alleged key manipulation operation is consistent across all embodiments.

Specifically with respect to the embodiment relied upon by the Examiner (embodiment 10), Matsuda describes "extracting a key ... from each record of the ... target file ... [that has been] ... stored in ... main memory" (Matsuda at 6:52-54), "adding a serial number or relative position data of a record having the key to the key" (Matsuda at 6:55-57), using the (modified) key value to obtain data, performing a operation on the obtained data based on a specified command and storing the data (Matsuda at 6:58-64).

It is significant to note that *nowhere* does Matsuda teach, describe or even suggest the use of variable length keys. To the contrary, because Matsuda describes adding an offset to an initial key value to obtain an address from which data is obtained (with no additional teaching), it is not believed possible for Matsuda to use variable length keys. If this were not so, there would be no way to uniformly generate a fixed length address. See, for example, Matsuda's detailed description of key extraction and manipulation operations with respect to FIGS. 1 (8:64-9:8 in which it is explicitly noted

that key fields are a constant length) and 3 (9:66-10:6 in which an illustrative size of the fixed length key fields are specified).

The Examiner's application of Matsuda to the claimed invention appears to confuse and conflate the difference between a value's magnitude (*e.g.*, 10 versus 100) and the LENGTH of the type of value (*e.g.*, a 16, 32 or 64-bit integer). In the field of computer science, a value type (*e.g.*, an integer or floating point) is separate and distinct from a value's magnitude (*e.g.*, 14 or 36.8). In practice, when an operation on two values results in a new value that is either too small or to large for the original value to represent, an error condition is generated (*i.e.*, underflow and overflow conditions). *Specifically, adding an offset to a fixed length key in accordance with Matsuda would not be expected to change the type and, therefore, LENGTH of the resulting value. Further, and more to the point, Matsuda does not teach, describe or even suggest that such is the case.*

2. Discussion

As acknowledged by the Examiner, AAPA does not teach, describe or even suggest techniques to avoid the use of intermediate storage for expanded key values. Office Action at page 5 (¶ 5). While Assignee does point out significant drawbacks to the described prior art techniques (Specification at paragraph 0003), *such a description does not constitute an admission that these drawbacks were recognized by others in the field or that other prior art sorting technologies were designed to mitigate these drawbacks.*

As noted above, nowhere does Matsuda teach, describe or even suggest the use of variable length keys – absent from Matsuda is any mention of variable length keys or any operations that are necessary to process variable length keys. In so far as this element of the claimed invention is totally missing from Matsuda, it is suggested and believed that AAPA (including FIG. 1) fairly describes the sort operation of Matsuda.

Even if Matsuda teaches what the Examiner alleges, there is absolutely no justification (implicit or explicit) for combining the cited references. Absent this, or

personal knowledge by the Examiner that justifies such a combination, the law (*e.g.*, *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308 (Fed. Cir. 1999); *In re Roufett*, 149 F.3d 1350, 1357 (Fed. Cir. 1998); *Ex parte Levengood*, 28 U.S.P.Q.2d (BNA) 1300 (Bd. Pat. App. & Inter. 1993); and *In re Mills*, 916 F.2d 680, 682 (Fed. Cir. 1990)) and Patent Office rules of practice (*e.g.*, M.P.E.P. 2143.01) are clear: the references cannot be combined. If the Examiner is relying on personal knowledge that one of ordinary skill in the art would have combined the cited references as alleged, the Examiner is requested to provide an Affidavit so stating in accordance with 37 C.F.R. 1.104(d)(2) and M.P.E.P. 2144.03.

For at least these reasons the combination of AAPA and Matsuda (alone or together) fails to render obvious the inventions recited in independent claims 1, 16, 27 and 40. As a result, the Examiner has failed to present a legitimate *prima facie* obviousness rejection under 35 U.S.C. 103. Accordingly, it is respectfully requested that the Examiner withdraw this rejection.

In addition, each of rejected claims 2-12, 17-24, 28-37 and 41-52 depend from one of independent claims 1, 16, 27 and 40. Since each independent claim is patentable as discussed above, each of the identified dependent claims are also allowable. Accordingly, it is respectfully requested that the Examiner withdraw this rejection.

Section 103 Rejections based on Applicants Admitted Prior Art, Matsuda et al. and Ferguson et al.

The Examiner has rejected claims 13-15, 25, 26, 38, 39 and 53-63 as allegedly being unpatentable under 35 U.S.C. 103(a) over AAPA in view of Matsuda and further in view of U.S. Patent 5,274,805 to Ferguson et al. (hereinafter Ferguson). Specifically, the Examiner asserts that:

> With respect to independent claim 55, AAPA teaches all of the claimed elements except "wherein the expanded key information is not stored in intermediate storage[,] repeating ... merging ... [and] ... reloading." Office Action at page 21 (¶ 6). The Examiner cites to Matsuda at Abstract and col. 6, lines 52-67 and Figure 2, alleging that "[t]hese lines and

fig 2 discloses the extraction and expansion of the key fields by adding the addresses of main memory. These expanded keys are not being stored in any intermediate storage but are being stored in the main memory." Office Action at page 21 (¶ 6). The Examiner relies of Ferguson for teaching the claimed acts of repeating (Ferguson at 5:24-40), merging (Ferguson at 3:18-27 and reloading (Ferguson at 9:64-10:4). Office Action at pages 22-23 (¶ 6). The Examiner concludes by stating "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because Ferguson's teaching would have allowed AAPA and Matsuda to require fewer storage system access [sic] an hence is generally faster."" Office Action at page 23 (¶ 6).

1. U.S. Patent 5,274,805 to Ferguson et al. ("Ferguson")

As noted in Assignee's prior Reply, Ferguson appears to be directed to "sorting and compressing data that has particular advantages in implementing a key index tree structure." Ferguson at 1:15-17. More specifically, sort methods in accordance with Ferguson use "substrings to sort strings of key records into a linked list structure that can be directly transformed into an index tree." Ferguson at 4:39-41. In Ferguson, sorting "is carried out in two phases, consisting of a pre-sort phase (similar to the prior art), followed by one or more merge passes that take advantage of the concept of a 'substring'." Ferguson at 7:4-7.

"In the pre-sort phase, a file of data records on a storage system is read and key records are extracted in known fashion ... sorted [and] ... written back to the storage system ... [where] ... as the sorted key records are written out onto the storage system, a 'substring field' is inserted at intervals in the data string to delimit the output string into substrings." Ferguson at 7:8-30. See also Ferguson at 14:50-15:2 and FIG. 9 (elements 90-94). During the merge phase, "[s]ubstrings are read from the storage system into associated input buffers reserved in the computer memory." Ferguson at 8:34-36. "Merge comparisons are performed on the contents of input buffer[s], ... with the sorted output records being stored in the output buffer. When the output buffer becomes full, it is written out to" storage. Ferguson at 8:67-9:4; see also FIGS. 3-5.

2. Discussion

As with Matsuda, nowhere does Ferguson teach, describe or even suggest the use of variable length keys – absent from Ferguson is any mention of variable length keys or any operations that are necessary to process variable length keys. Further, the *combination* of Matsuda and Ferguson fail utterly to suggest that either be used to process variable length key information and, as a consequence, fail to teach all of the claimed elements. It is noted that a combination rejection requires three elements: (1) there must be some suggestion or motivation to make the combination; (2) there must be a reasonable expectation of success; and (3) the prior art references must teach or suggest all the claimed elements. *In re Vaeck*, 947 F.2d 488, 493 (Fed. Cir. 1991); M.P.E.P. 2143.

It appears the Examiner is using the drawbacks to prior art techniques *identified by the Assignee* (see discussion above regarding Matsuda) as a guide to justify combining the cited references. Such conduct is expressly prohibited by law and Patent Office rules of practice. *In re Roufett*, 149 F.3d 1350, 1357 (Fed. Cir. 1998) (motivation to combine is required because without it, "rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be an illogical and inappropriate process by which to determine patentability.") (citation omitted); M.P.E.P. 2143.01 ("The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination," quoting *In re Mills*, 916 F.2d 680, 682 (Fed. Cir. 1990).

For at least these reasons the combination of AAPA, Matsuda and Ferguson (alone or together) fails to render obvious the invention recited in independent claim 55. As a result, the Examiner has failed to present a legitimate *prima facie* obviousness rejection under 35 U.S.C. 103. Accordingly, it is respectfully requested that the Examiner withdraw this rejection.

In addition, each of rejected claims 13-15, 25, 26, 38, 39, 53, 54 and 56-63 depend from one of independent claims 1, 16, 27, 40 and 55. Since each independent claim is patentable as discussed above, each of the identified dependent claims are also allowable. Accordingly, it is respectfully requested that the Examiner withdraw this rejection.

CONCLUSIONS

Reconsideration of pending claims 1-63 in light of the above remarks is respectfully requested. If, after considering this reply, the Examiner believes that a telephone conference would be beneficial towards advancing this case to allowance, the Examiner is strongly encouraged to contact the undersigned attorney at the number listed.

/Coe F. Miles, Ph.D., J.D./ Date: 11 July 2006
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